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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,554	08/30/2001	Leonard Forbes	1303.028US1	1837

21186 7590 10/22/2003

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,554	FORBES, LEONARD	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- Th MAILING DATE of this communication app ars on the cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,19-27,29-44,46-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,11,12,37,38,43,44 and 46-49* is/are allowed.

6)☒ Claim(s) *1-6,9,10,19-21,24,25,29,30,33-36,39 and 40* is/are rejected.

7)☒ Claim(s) *22,23,26,27,31,32,41 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on August 1, 2003 has been entered.

Information Disclosure Statement

2. The Information Disclosure Statement filed on August 1, 2003 has been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,2,3,4,5,6,9,10,19-21,24,25,29,30,33-36,39, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over FORBES ET AL. (6,141,248) in view of GARDNER ET AL. (6,210,999).

Forbes et al. discloses a memory cell, or a method for making the same, with a pair of cross coupled inverters 206-308 and 210-312, wherein each inverter includes an NMOS transistor 308,312 and a PMOS transistor 206,210, and wherein at least one of the NMOS transistors 308,312 includes: a first source/drain region 118 and a second source/drain region 122 separated by a channel region 120a in a substrate 120; a floating gate 116 opposing the channel region 120a and separated therefrom by a gate oxide 126; and a control gate 114 opposing the floating gate 116, wherein the control gate 114 is separated from the floating gate 116 by a intergate insulator 124; and a conformal method of forming said memory cell, comprising: forming the said pair of cross coupled inverters 206-308 and 210-312, wherein forming each said inverter includes an NMOS transistor 308,312 and a PMOS transistor 206,210, and wherein the method includes forming at least one of the NMOS transistors 308,312 to include: the said first source/drain region 118 and the said second source/drain region 122 separate by the said channel region 120a in the said substrate 120; the said floating gate 116 opposing the said channel region 120a and separated therefrom by the said gate oxide 126; and the said control gate 114 opposing the said floating gate 116, wherein the said control gate 114 is separated from the said floating gate 116 by the said intergate insulator 124. With regard to claims 2,9,10,19-21,24,25,29,30,33-36,39,40 Forbes et al. discloses a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors; and wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry. With further

regard to claims 19-21,24,25,29-30 and 39-40 Forbes et al further discloses a wordline coupled to the pair of access transistors. With further regard to claims 29-30 Forbes et al further discloses a processor, and a memory device coupled to the processor, wherein the memory device includes an array of the above described memory cells. Note figures 5B and 8A and column 5 lines 1-60 of Forbes et al. Forbes et al. does not disclose that the intergate insulator is a low tunnel barrier intergate insulator comprising, according to claims 3-6, 10,21,34-36, and 40 any of a transition metal oxide is selected from the group consisting of Ta_2O_5 $Ti0_2$ ZrO_2, and Nb_2O_5, a Perovskite oxide, PbO, or Al_2O_3.

However Gardner et al. discloses a memory cell including at least one NMOS transistor wherein the NMOS transistor includes an intergate insulator 60 comprising any of transition metal oxide Ta_2O_5, Perovskite oxide BST, and Al_2O_3. Note figure 17 and column 10 lines 65-67, column 8 lines 25-40, and column 4 lines 9-17 of Gardner et al. Note that Gardner et al.'s intergate insulator is formed by sputtering at low temperatures. Applicant reports that an inherent property of low-temperature sputtered Ta_2O_5, Perovskite oxide, and Al_2O_3 intergate insulators is that they have low tunnel barriers. Note application, pages 26-30, and 32. Therefore, it would have been obvious to a person having skill in the art to replace the intergate insulator of Forbes et al.'s memory cell with the transition metal oxide Ta_2O_5, Perovskite oxide BST, or Al_2O_3 low tunnel barrier intergate insulator such as taught by Gardner et al. (note that Gardner et al. does not consider the low tunnel barrier property important enough to mention, it is simply inherent) in order to increase the control gate ca-

pacitance without requiring that the intergate insulator be thinned to the point where breakdown becomes a hazard. Note column 2 lines 7-57 of Gardner et al.

Allowable Subject Matter

4. Claims 7,8,11,12,37,38,43,44, and 46-49 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a memory cell comprising a pair of cross coupled inverters, wherein each inverter includes at least one NMOS transistor with a floating gate including a polysilicon floating gate having a metal layer formed thereon in contact with a low tunnel barrier intergate insulator as recited in claims 7,11, and 37, or wherein the control gate is the gate having a metal layer formed thereon in contact with a low tunnel barrier intergate insulator as recited in claim 8, or such as a method for operating an SRAM cell which includes a pair of cross coupled floating gate transistors, comprising writing to at least one of the cross coupled floating gates of the SRAM cell using channel hot electron injection, wherein the cross coupled floating gate transistors each include: a first source/drain region and a second source/drain region separated by a channel region in a substrate; a floating gate opposing the channel region and separated therefrom by a gate oxide; and a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate; sensing a logic state of the SRAM cell in a

start up mode, and writing to the floating gate by tunneling electrons from the control gate to the floating gate, as recited in claim 43.

5. Claims 22,23,26,27,31,32, 41, and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
10/2003

Minhloan Tran
Primary Examiner
Art Unit 2826